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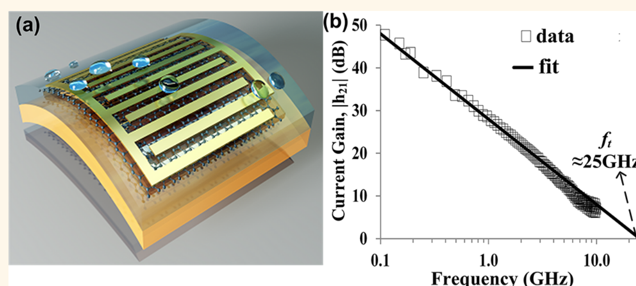
25 GHz Embedded-Gate Graphene Transistors with High-K Dielectrics on Extremely Flexible Plastic Sheets

Jongho Lee,[†] Tae-Jun Ha,[†] Huifeng Li,[‡] Kristen N. Parrish,[†] Milo Holt,[†] Ananth Dodabalapur,[†] Rodney S. Ruoff,[‡] and Deji Akinwande*[,†]

[†]Department of Electrical and Computer Engineering,The University of Texas at Austin, Austin, Texas 78758, United States and [‡]Department of Material Science and Engineering,The University of Texas at Austin, Austin, Texas 78758, United States. The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

ABSTRACT Despite the widespread interest in graphene electronics over the past decade, high-performance graphene field-effect transistors (GFETs) on flexible substrates have been rarely achieved, even though this atomic sheet is widely understood to have greater prospects for flexible electronic systems. In this article, we report detailed studies on the electrical and mechanical properties of vapor synthesized high-quality monolayer graphene integrated onto flexible polyimide substrates. Flexible graphene transistors with high-k dielectric afforded intrinsic gain, maximum carrier mobilities of 3900 cm^2/V·s, and importantly, 25 GHz cutoff frequency, which is more than a factor of 2.5 times higher than prior results. Mechanical studies reveal robust transistor performance under repeated bending, down to 0.7 mm bending radius, whose tensile strain is a factor of 2–5 times higher than in prior studies. In addition, integration of functional coatings such as highly hydrophobic fluoropolymers combined with the self-passivation properties of the polyimide substrate provides water-resistant protection without compromising flexibility, which is an important advancement for the realization of future robust flexible systems based on graphene.



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Two-dimensional (2D) atomic sheets such as graphene are widely considered to have considerable prospects for future flexible smart electronic systems owing to their large breaking strength afforded by the strong in-plane sigma (σ) bonds,[1,2] large surface area for sensing,[3,4] high carrier mobilities which can exceed 10,000 cm^2/V·s at room temperature,[5,6] electron–hole symmetry for frequency translation which is essential for communication systems,[7–9] and notably, very high cutoff frequencies which have been demonstrated to exceed 100 GHz on hard conventional substrates.[10,11] The high-frequency property is a particularly important feature for flexible electronics which has historically been restricted to low sub-GHz frequencies owing to the slow carrier transport in contemporary flexible devices made from organic semiconductors and amorphous silicon.[12]

However, despite the device demonstrations of high-frequency graphene field-effect transistors (GFETs) on conventional hard substrates, similar frequency performance has not been previously achieved on flexible substrates owing to the more complex material integration, device fabrication, and challenges associated with controlling the interfacial properties of the flexible substrate including surface smoothness and heat management.[7,13,14]

In this article, we report a flexible graphene transistor with cutoff frequency of 25 GHz, which is more than a factor of 2.5 times higher than that for previously reported GFETs on flexible substrates (Figure 2d).[14–16] This is enabled by the (i) development of a gate-first device structure where the complex fabrication and high-k dielectric integration are realized before graphene transfer and (ii) integration of high-quality Cu-catalyzed

* Address correspondence to: deji@ece.utexas.edu.

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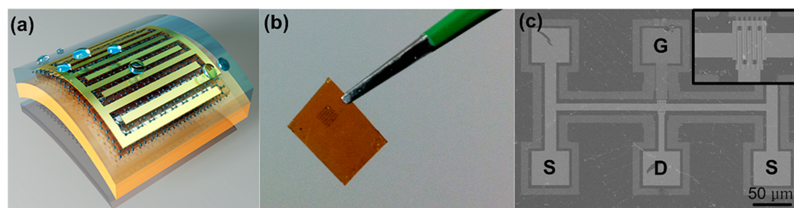

Figure 1. Flexible graphene field-effect transistors. (a) 3-D illustration of a water-resistant flexible multifinger embedded-gate GFET. (b) Optical image of the flexible substrate with an array of graphene transistors. (c) Scanning electron microscope image of the GFET with a ground-signal-ground pad configuration for RF characterization. (Inset) Channel area with multifinger electrodes of six fingers.

chemical vapor deposited (CVD) graphene onto a smooth dielectric interface for optimum carrier transport. The latter employs graphene of high material quality on a smooth surface to ensure optimum carrier transport, while the former is a practical route in reducing fabrication-related graphene damage which has been widely reported.[17−20] Furthermore, electromechanical studies demonstrate robust device performance, which is enabled by preparing local dielectric islands for graphene channels, down to a 0.7 mm bending radius, whose tensile strain is a factor of 2−5 times higher than prior GFETs with low bending radius (Figure 3d).[14,15,20,21] In addition, we integrate functional coatings such as highly hydrophobic fluoropolymers which afford water-resistant protection, a desirable attribute for future flexible electronic systems that are reliable in dry and temporary aqueous conditions.

Figure 1a is a 3-D illustration of a water-resistant GFET. Figure 1b is an optical image of the fabricated free-standing polyimide (PI) film with an array of flexible graphene devices. PI film (100 μm thick) is utilized as the flexible substrate due to its robust thermal (high glass transition temperature) and mechanical properties along with compatibility to most chemicals used during microelectronic lithographic processes.[20] The substrate was cured under nitrogen atmosphere as described in a prior work.[7,13,20]

RESULTS

Figure 2 shows the electrical properties of the GFETs evaluated at room temperature under ambient conditions. The gate modulation over the total resistance including contributions from the graphene channel and the metal contacts from the device are shown in Figure 2a. Figure 2b shows the drain current and the transconductance at different gate biases while the drain bias is fixed at 10 mV. Experimental data have good agreement with a widely used low-field diffusive transport model for graphene transistors.[22] The peak carrier mobility of 3900 $cm^2/V \cdot s$ from the device is measured and confirmed with the device model. The asymmetry in the carrier transport comes from the use of high work-function metal as electrodes, which favors hole transport while introducing additional junction resistances for electron transport.[20] Compared to a device fabricated with a lithography-free process (mobility 8000 $cm^2/V \cdot s$, see Figure S2 of Supporting Information [SI]), the patterned device reported here showed carrier mobility degradation due to impurity scattering from the undesirable resist residue left on the graphene channel,[23] which requires further studies on an efficient resist removal and surface cleaning process compatible with flexible substrates. Nonetheless, mobilities above 2000 $cm^2/V \cdot s$ are sufficient for high-frequency graphene devices.[11]

DISCUSSION

A central motivation for exploring graphene is its high-speed charge transport which can enable RF and high-frequency electronic applications on flexible substrates. In this light, we experimentally evaluated its scattering parameters (S-parameters) to determine the current gain (h_{21}) and cutoff or transit frequency (f_T) which is a key metric of device speed.[10,11,24] The as-measured S-parameters typically include delay contributions from parasitic capacitance and interconnect resistance that prevent direct evaluation of the intrinsic speed of charge carriers.[24] The parasitic components arise from the metal electrodes used in the RF device structure shown in Figure 1c. In the presence of these parasitics, the measured transit frequency is referred to as the extrinsic transit frequency ($f_{T,ext}$) and is given by $f_{T,ext} = G_m/[2\pi(C_{gc}+C_{par})]$, where G_m is the extrinsic transconductance which includes the impact of the parasitic electrode resistances, C_{par} is the sum of the parasitic capacitances between electrodes, and C_{gc} is the gate to channel capacitance which includes the gate oxide and the quantum capacitance contributions (see Figure S1 of SI for illustration of the device cross section). On the other hand, the intrinsic $f_T = g_m/2\pi C_{gc}$, where g_m is the (intrinsic) transconductance without parasitic resistance effect and always satisfies the condition $g_m \geq G_m$. As such, $f_{T,ext}$ can be substantially less than f_T by orders of magnitude.[10,25] For this reason, the presence of parasitic resistances and capacitances obscures direct evaluation of the intrinsic carrier speed in nanomaterials and devices.

In order to overcome this limitation, we employ the standard two-step de-embedding method that

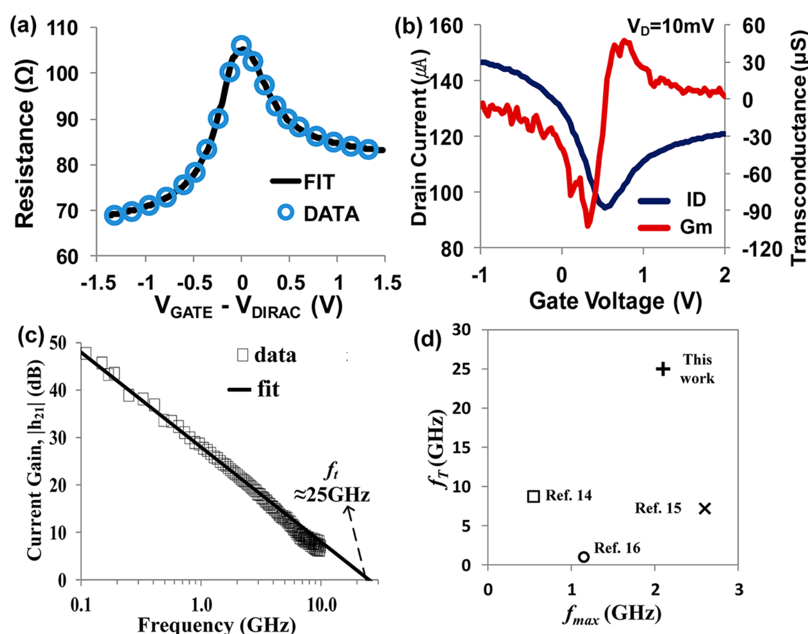

Figure 2. Electrical measurements. (a), (b) Gate modulation from the device showing the carrier mobility of 2800 $cm^2/V \cdot s$ for hole transport and 3900 $cm^2/V \cdot s$ for electron transport, respectively. The device has a channel length of 0.5 μm, and an effective channel width of 100 μm. V_D = 10 mV. (c) The de-embedded current gain with an intrinsic f_T of 25 GHz for flexible GFET. V_G is biased at the peak transconductance and V_D = 0.5 V. All measurements were performed at room temperature under ambient condition. (d) Comparison of the intrinsic f_T vs. f_{max} (with the exception of ref 15. which reported extrinsic values). The flexible GFETs have comparable channel lengths of 0.5 μm except for ref 14., which has the channel length of 0.17 μm.

involves measurement of so-called open and short test structures which are identical to the device structure and fabricated on the same substrate but without the graphene active layer. Essentially, the two-step method consists of first measuring the extrinsic device response; afterward, the open and short test structures are measured in order to subtract out the parasitic capacitance and resistance effect.[11,24] The intrinsic current gain is shown in Figure 2c revealing $f_T \approx 25$ GHz, the highest cutoff frequency for flexible GFET to date (see Figure 2d). The experimental de-embedded value is in good agreement with an analytical estimate of ~30.9 GHz (see SI for analysis details). The extracted flexible GFET f_T is about 50% lower than the highest reported GFET of similar channel length (0.55 μm) on conventional hard substrates,[11] albeit the drain voltage (0.5 V) of our flexible GFET is a quarter of that on the hard substrate (2 V).[11] The low thermal conductivity and glass transition temperature of plastic sheets are barriers that prematurely restrict the fields and current densities necessary to probe the ultimate cutoff frequency on flexible substrates.[7,15] Basic exploration of heat management materials (such as hexagonal boron nitride and other suitable thin films) is a matter of critical importance for advanced flexible electronics and warrants awareness and further studies. A higher drain voltage is expected to afford commensurate improvement in the cutoff frequency.[11] An $f_{max} \approx$ 2.1 GHz was extracted from Mason's unilateral gain (Figure S4 of SI). The relatively low f_{max} is due to the well-recognized impact of unoptimized gate-metal resistance and gate-drain coupling capacitance.[24,26] Applied research utilizing self-aligned T-gate structures on flexible substrates is desirable to achieve substantial improvement in f_{max}.[27,28]

MECHANICAL FLEXIBILITY

The mechanical flexibility of the device was evaluated with custom-designed bending test fixtures. In order to achieve high flexibility, the rigid components (electrodes and gate dielectrics) integrated in the device have to be patterned properly. While unpatterned devices only survive the maximum bending radius of 2 mm, which corresponds to ~3% tensile strain mostly due to the dielectric breakdown,[20] the patterned devices can survive bending down to a radius of 0.7 mm, which corresponds to ~8.6% strain. Hence, dielectric patterning is critical in order to avoid premature failure owing to crack propagation in the dielectric layer, which would limit the prospect of achieving a low bending radius. (See Figure S5 of SI. The device in this study has a small dielectric island with a thin Al_2O_3 dielectric.) The tensile strain (ε) is computed according to the relation $\varepsilon = t_s/(2R_B)$ where t_s and R_B are the substrate thickness and bending radius, respectively.[15,29] Figure 3a shows the flexible substrate with fabricated GFETs mounted on the custom-designed bending fixture. During the measurements, the normalized resistance from the metal contacts and the normalized mobility extracted from the device model have been monitored as shown in Figure 3b; no noticeable degradation was observed

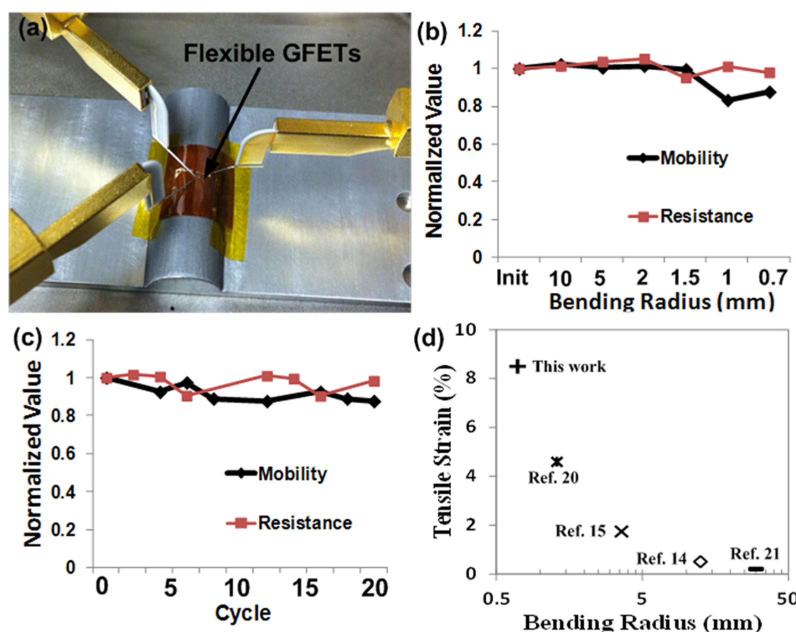

Figure 3. Mechanical bending measurements. (a) Flexible GFETs attached to the bending fixture. (b) The change in normalized resistance and normalized mobility under different bending radii down to 0.7 mm. (c) Repeated measurements of normalized resistance and normalized mobility at the minimum bending radius of 0.7 mm. Devices are biased at V_D = 10 mV for all these measurements. (d) Tensile strain vs bending radius from previously reported flexible GFETs with solid-state gate dielectrics.

from the resistance. The mobility remains over 80% compared to the value at the flat condition at the minimum bending radius of 0.7 mm. Repeated measurements under the minimum bending radius shown in Figure 3c confirm the reliability of the graphene device structure. At a lower bending radius, we observe mechanical breakdown of the gate dielectric, which compromises the dielectric capacitance and leads to high gate leakage (see Figure S5 of SI); however, the metal electrode is structurally intact and remains conductive.[20]

ENCAPSULATION FOR WATER-RESISTANT APPLICATIONS

The effective encapsulation and protection of the flexible GFET by a hybrid bilayer (inorganic/organic) coating against liquid exposure (DI water) has been confirmed both by the static contact angle measurements and by the electrical measurements. The FTA200 contact angle goniometer is used to measure the contact angles for different passivation materials investigated, including bare PI films, cured PI films, PECVD Si_3N_4, and CYTOP coating on the flexible devices. The fabricated sample was self-passivated at the back-side by the bare PI substrate, while the top-side of the device was implemented on the smooth, cured PI surface and passivated by Si_3N_4/CYTOP bilayer.

Figure 4a shows the optical images captured by the optical microscope attached to the goniometer. During the measurement, 20 μL of DI water is dropped on each surface. Bare PI films offer high hydrophobicity with a high contact angle of 82.5°, which affords good protection to DI exposure. However, the bare PI film is not recommended for integrated graphene devices due to the surface roughness and requires the coating/curing process to smoothen the surface.[20,30] After the spin-coated smoothing layer is cured, the hydrophobicity of the PI surface is slightly reduced down to 79.2°. Si_3N_4 does not improve the hydrophobicity, although it does provide outstanding mechanical robustness even under extreme static loading conditions.[20] Of the different coating films investigated in this work, we identified highly hydrophobic CYTOP, which offers a high contact angle exceeding 110°, as the most suitable water protection layer.

Parts b−e of Figure 4 present the electrical measurements under DI water exposure; b and c of Figure 4 are the data from Si_3N_4 passivated devices and d and e of Figure 4 are the data from the bilayer (Si_3N_4/ CYTOP) passivated devices. The devices were dipped into DI water for 10 s, dried with N_2 flow, and repeatedly measured. To evaluate the short-term protection against DI water immersion, the measurements were repeated up to 150 s while monitoring the changes in the normalized resistance and the carrier mobility. As for the long-term DI water exposure, the same measurements were performed after immersion for 2 days. The dotted lines in Figure 4b−e represent the virtual boundary between short-term measurements and long-term measurements. The normalized resistance does not show any noticeable degradation for both cases, while the carrier mobility degraded significantly for nitride passivated devices down to 30% of the initial value. This reduction in the mobility is due to nonideal

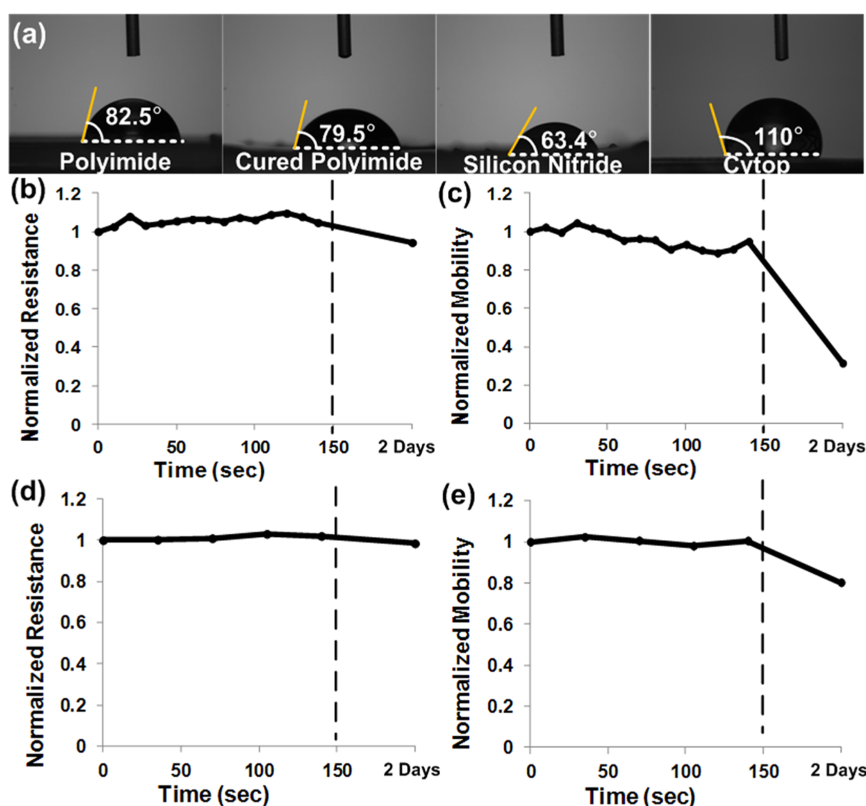

Figure 4. Immersion test results. (a) Contact angle measurements: 20 μL DI water dropped on prepared samples including as-received commercial polyimide film, cured polyimide film, PECVD Si_3N_4, and Cytop coated on Si_3N_4/PI. (b−e) Normalized resistance and mobility. Data shown on the left side of the dashed line are for short-term exposure to DI water, and data on the right side of the line are for long-term exposure to DI water. (b, c) Normalized resistance and mobility measured from Si_3N_4 passivated devices. (d, e) Normalized resistance and mobility measured from Cytop/Si_3N_4 passivated devices.

water protection from the nitride passivation layer. A low contact angle (less hydrophobic surface) of the layer allows water molecules to wet the surface and eventually introduces carrier traps in the dielectric interfaces, hence, weakening the gate modulation. The bilayer coated device shows no degradation of its resistance and slight degradation of its mobility, while providing 80% of the initial electrical performance. The improved water-resistant protection is attributed to the strong hydrophobic surface of CYTOP. This result suggests that functional coatings can be employed to protect flexible GFETs from water or liquid exposure, which is anticipated as a future requirement for robust flexible smart systems.

CONCLUSIONS

To summarize, we implemented high-performance graphene field-effect transistors on flexible PI substrates. A high mobility of 3900 $cm^2/V\cdot s$ is achieved for the multifinger embedded-gate flexible GFET. The fabricated multifinger device affords a cutoff frequency of 25 GHz and mechanical robustness down to a bending radius of 0.7 mm. The functional bilayer coating consisting of inorganic and organic thin films provides an effective hydrophobic surface offering water-resistant protection and reliable electrical functionality under short-term and relatively longer-term exposure to DI water.

METHODS

Graphene Field-Effect Transistors Fabrication. The devices are implemented as follows. The first EBL patterned an array of gate electrodes directly on prepared flexible substrates; Ti/Pd (2 nm/48 nm) was deposited as gate electrodes. Multifinger electrodes up to 10 fingers were patterned to enhance the current drive.[20] A high-k dielectric of 10-nm thick Al_2O_3 was deposited by atomic layer deposition (ALD) and patterned by the second EBL and subsequent wet-etch using a 1:3 diluted solution of H_3PO_4:DI water. The gate pad was opened during this process, and the patterned dielectric island with an estimated gate-oxide capacitance of 600 nF/cm^2 works as the gate dielectric offering a planar surface where the graphene channel is placed. CVD monolayer graphene film was then transferred on to the patterned device *via* the conventional poly(methyl methacrylate) (PMMA) assisted wet-transfer process using ammonia persulfate to etch the supporting copper foil.[31] The third EBL process and oxygen plasma patterned the graphene film into active channels. Source and drain electrodes (2 nm Ti/50 nm Au) were defined by the EBL and thermal evaporation to complete the basic device

structure. A bilayer of inorganic and organic films was deposited to completely passivate the device. The top side of the device was first covered with a 30-nm-thick low-power nitrogen-rich plasma-enhanced chemical vapor-deposited (PECVD) silicon nitride to provide mechanical robustness with no noticeable degradation in the electrical performance.[20,32] The redundant area of silicon nitride on the metal probe pads and the boundary of devices are patterned by the additional EBL process and the dry-etch of silicon nitride by CF_4 RIE with the etch rate of 150 nm/min. Finally, the sample was coated with CYTOP fluoropolymer.[33] A diluted CYTOP solution was formed using the as-supplied CYTOP and CYTOP solvent from Asahi Glass Co. (CYTOP:CYTOP solvent = 1: 10) with magnetic stirring for ∼10−12 h in an inert environment. CYTOP, as a 90-nm thick layer, was deposited by spin-coating a diluted CYTOP solution on silicon nitride passivated devices. After the coating, the samples were cured by gradually increasing the annealing temperature from 30 to 225 °C for over an hour under nitrogen atmosphere. The CYTOP cover layer is left unpatterned due to its mechanical softness allowing direct probe-tip measurements.

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: The multimedia video file of the immersion tests with the fluoropolymer coated GFET. Figure S1: the illustration of the device. Figure S2: electrical measurements of the device fabricated with the lithography-free process. Figure S3: the extrinsic and intrinsic cutoff frequency measured from the device. Figure S4: the power-gain frequency measured from the device. Figure S5: the bending tests of MIM (metal−insulator−metal) capacitors on flexible polyimide substrate. Figure S6: the dependence of GFET transfer characteristics on mechanical bending. Figure S7: the statistical data for the immersion tests. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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